ABSTRACT OF THE DISCLOSURE

A self-timed scan circuit includes a multiplexer for selecting either a data input or a test input in response to an internal test enable signal and for generating a multiplexed output; a latch coupled to the multiplexer for generating a latched output in response to a next clock pulse; and a timing control circuit for generating the internal test enable signal in response to a global test enable signal wherein the internal test enable signal is set to logic one when the global test enable signal is set to logic one and wherein the internal test enable signal is set to logic zero in response to the next clock pulse.